region. This can be done by locally diffusing a lifetime-killing impurity such as platinum into the central region **81** of the P type gate layer **12** or by suitably locally irradiating this region. Either of these techniques, which are also described in my U.S. Pat. No. 5,005,065, can be used alone or in combination with the techniques described in the two immediately-preceding paragraphs.

While particular embodiments of the invention have been shown and described, it will be obvious to those skilled in the art that various changes and modifications may be made without departing from the invention in its broader aspects; and it is therefore intended herein to cover all such changes and modifications as fall within the true spirit and scope of the invention.

What is claimed as new is:

1. A MOS-controlled thyristor comprising:

(a) a multi-layer semiconductor body having at least four layers, with contiguous layers being of different P and N conductivity types and with at least three back-to-back PN junctions between contiguous layers; one end layer constituting an anode layer, an opposite end layer constituting a cathode layer, and an intermediate layer contiguous with said cathode layer constituting a gate layer; said cathode layer being divided into many elongated fingers, thereby dividing the PN junction between said cathode layer and said gate layer into many discrete PN subjunctions between said fingers and said gate layer which are effectively in parallel which each other so as to share the current through said thyristor when said thyristor is "on"; said gate layer having predetermined surface regions adjacent said cathode layer but uncovered by said cathode-layer fingers and respectively surrounding the PN subjunctions between said fingers and the gate layer;

(b) an anode electrode in ohmic contact with said anode layer,

(c) a cathode electrode having portions respectively registering with and in ohmic contact with said fingers,

(d) a gate electrode in ohmic contact with said gate layer in said predetermined surface regions of said gate layer, said gate electrode surrounding the PN subjunctions between said fingers and the gate layers, and

(e) a MOS field-effect transistor connected between said cathode electrode and said gate electrode and being located in a separate area of the thyristor from said fingers, said MOS field-effect transistor having a high-resistance state when the thyristor is "on" and being switchable into a low-resistance "on" state, thereby developing a low-resistance bypass around said PN subjunctions and turning off said thyristor upon being switched into said low-resistance "on" state.

2. The thyristor of claim **1** in which one or more additional field-effect transistors having a high-resistance state when the thyristor is "on" are connected between said cathode electrode and said gate electrode and are located in separate areas of the thyristor from said fingers, said field-effect transistors being switchable substantially in unison into a low-resistance "on" state, thereby developing a low resistance bypass around said PN subjunctions and turning off said thyristor upon being switched into said "on" state.

3. A thyristor comprising:

(a) a multi-layer semiconductor body having at least four layers, with contiguous layers being of different P and N conductivity types and with at least three back-to-back PN junctions between contiguous layers; one end layer constituting an anode layer, an opposite end layer

constituting a cathode layer, and an intermediate layer contiguous with said cathode layer constituting a gate layer; said cathode layer being divided into many elongated fingers, thereby dividing the PN junction between said cathode layer and said gate layer into many discrete PN subjunctions between said fingers and said gate layer which are effectively in parallel with each other so as to share the current through said thyristor when said thyristor is "on"; said gate layer having predetermined surface regions adjacent said cathode layer but uncovered by said cathode-layer fingers and respectively surrounding the PN subjunctions between said fingers and the gate layer;

(b) an anode electrode in ohmic contact with said anode layer,

(c) a cathode electrode having portions respectively registering with and in ohmic contact with said fingers,

(d) a gate electrode in ohmic contact with said gate layer in said predetermined surface regions of said gate layer, said gate electrode surrounding the PN subjunctions between said fingers and the gate layer, and

(e) a solid-state switching device connected between said cathode electrode and said gate electrode and being located in a separate area of said thyristor from said fingers, said switching device having a high-resistance state when the thyristor is "on" and being switchable to a low-resistance "on" state, thereby developing a low-resistance bypass around said PN subjunctions and turning off said thyristor upon being switched into said low-resistance "on" state.

4. The thyristor of claim 3 in which said solid-state switching device has a resistance in its "on" state sufficiently low to divert at least 10 percent of the anode current passing through said thyristor into one or more paths bypassing said subjunctions upon being switched into its "on" state.

5. The thyristor of claim 3 in which each of said PN subjunctions has a region located centrally of said subjunction that is characterized by a substantially lower avalanche voltage than characterizes the region of said PN subjunction that surrounds said centrally-located region.

6. The thyristor of claim 3 in which each of said PN subjunctions has a region located centrally of said subjunction that is characterized by an avalanche voltage at least 4 volts lower than characterizes the region of said PN subjunction surrounding said centrally-located region.

7. The thyristor of claim 3 in which each of said PN subjunctions has a region located centrally of said subjunction that is characterized by a lower electron-injection efficiency than characterizes the region of said subjunction that surrounds said centrally-located region.

8. The thyristor of claim 7 in which said gate layer includes in its region immediately adjacent said central region of each of said PN subjunctions a zone in which the conduction carriers present are characterized by having a lifetime substantially shorter than characterizes the conductive carriers present in the zone of said gate layer immediately adjacent the region of said PN subjunction that surrounds said centrally-located region.

9. The thyristor of claim 7 in which:

(a) the PN junction between said gate layer and an intermediate layer adjacent thereto constitutes a middle PN junction of the thyristor, and

(b) most of the central region of each subjunction is located a greater distance from said middle PN junction of the thyristor than is the region of said PN subjunction that surrounds said central region.

9

10. The thyristor of claim 3 in which:

(a) aligned with each subjunction, the gate layer has a portion projecting from the surface of the gate layer that is in ohmic contact with said gate electrode, and

(b) one said cathode layer fingers is located at the outer end of each said projecting portion.

11. A MOS-controlled thyristor, comprising:

(a) a thyristor in the form of a multi-layer semiconductor body having anode, cathode and gate electrodes in ohmic contact with respective layers of said multi-layer semiconductor body, and having on and off states of respective conduction and non-conduction of current therethrough for high-power switching by said thyristor; and

(b) a discrete MOSFET transistor having gate, source and drain electrodes and having a low-resistance on state and a high-resistance off state controlled by a predetermined voltage signal applied to the gate electrode of said MOSFET transistor to respectively enable and disable current flow through a source-drain path thereof, said source and drain electrodes being electrically connected between one of said cathode and anode electrodes and said gate electrode of said thyristor, whereby said thyristor is controllable to be turned from its on state to its off state by switching said MOSFET transistor from its high-resistance off state to its low-resistance on state, respectively, said MOSFET transistor being separate from but in proximity to said multi-layer semiconductor body.

12. The MOS-controlled thyristor of claim 11, in which said MOSFET transistor is located on a major surface of said multi-layer semiconductor body.

13. The MOS-controlled thyristor of claim 11, in which plural MOSFET transistors are connected by electrical leads between said one of said cathode and anode electrodes and said gate electrode of said thyristor.

14. The MOS-controlled thyristor of claim 13, in which plural MOSFET transistors are located relative to said thyristor to render said electrical leads of near-minimum length.

15. The MOS-controlled thyristor of claim 13, in which said plural MOSFET transistors are operable to be switched simultaneously from the respective high-resistance off state to the respective low-resistance on state.

16. A process for fabricating a MOS-controlled thyristor, comprising the steps of:

(a) forming a high-power thyristor by process technology as a multi-layer semiconductor body

having multiple PN junctions and anode, cathode and gate electrodes in ohmic contact with respective layers of said multi-layer semiconductor body, to provide the thyristor with on and off states of respective conduction and non-conduction of current therethrough;

(b) fabricating at least one discrete MOSFET transistor using an integrated circuit fabrication process technology distinct from the steps of forming said thyristor, including providing said at least one MOSFET transistor with gate, source and drain electrodes for switching between a low-resistance on state and a high-resistance off state controlled by voltage applied to the gate electrode of said at least one MOSFET transistor;

(c) locating said at least one MOSFET transistor proximate said semiconductor body of said thyristor and electrically connecting said source and drain electrodes between one of said cathode and anode electrodes and said gate electrode of said thyristor, whereby to render said thyristor controllable to be turned from its on state to its off state by switching said at least one MOSFET transistor from its high-resistance off state to its low-resistance on state, respectively.

17. The process of claim **16**, including the step of locating said at least one MOSFET transistor on a major surface of said semiconductor body of said thyristor.

18. The process of claim **16**, including the steps of connecting plural MOSFET transistors fabricated by said integrated circuit process technology distinct from the process technology by which said thyristor is formed between said one of said cathode and anode electrodes and said gate electrode of said thyristor.

19. The process of claim **18**, wherein the step of connecting said plural MOSFET transistors between said one of said cathode and anode electrodes and said gate electrode of said thyristor includes locating each of said plural MOSFET transistors relative to said thyristor such that electrical leads connecting said plural MOSFET transistors between said one of said cathode and anode electrodes and said gate electrode of said thyristor are of near-minimum length.

20. The process of claim **18**, wherein the step of connecting said plural MOSFET transistors is performed to enable them to be switched simultaneously from the high-resistance off state to the low-resistance on state of the respective transistor, for turning said thyristor to its off state.

21. The MOS-controlled thyristor comprising:

(a) a thyristor in the form of a multi-layer semiconductor body having anode, cathode and gate electrodes in ohmic contact with respective layers of said multi-layer semiconductor body, and having on and off states of respective conduction and non-conduction of current therethrough for high-power switching by said thyristor; and

(b) a solid-state switching device connected between one of said anode and cathode electrodes and said gate electrode and being located in a separate area of said thyristor from said one of said anode and cathode electrodes, said switching device having a high-resistance state when the thyristor is "on" and being switchable to a low-resistance "on" state, thereby developing a low-resistance bypass around said multi-layer semiconductor body and turning off said thyristor upon being switched into said low-resistance "on" state.

22. The controlled thyristor of claim **21**, in which said solid-state switching device is located on a major surface of said multi-layer semiconductor body.

23. The controlled thyristor of claim **21**, in which a plurality of said switching devices are connected by electrical leads between said one of said cathode and anode electrodes and said gate electrode of said thyristor.

24. The controlled thyristor of claim **23**, in which said plurality of said switching devices are located relative to said thyristor to render said electrical leads of near-minimum length.

25. The controlled thyristor of claim **23**, in which said plurality of said switching devices are operable to be switched simultaneously from the respective high-resistance off state to the respective low-resistance on state.

26. A process for fabricating a controlled thyristor, comprising the steps of:

(a) forming a high-power thyristor by process technology as a multi-layer semiconductor body having multiple PN junctions and anode, cathode and gate electrodes in ohmic contact with respective layers of said multi-layer semiconductor body, to provide the thyristor with on and off states of respective conduction and non-conduction of current therethrough;

(b) fabricating at least one discrete solid-state switching device using an integrated circuit fabrication process technology distinct from the steps of forming said thyristor, said at least one solid-state switching device having a low-resistance on state and a high-resistance off state; and

(c) locating said at least one solid-state switching device proximate said semiconductor body of said thyristor and electrically connecting said at least one solid-state switching device between one of said cathode and anode electrodes and said gate electrode of said thyristor, whereby to render said thyristor controllable to be turned from its on state to its off state by switching said at least one solid-state switching device from its high-resistance off state to its low-resistance on state, respectively.

27. The process of claim **26**, including the step of locating said at least one solid-state switching device on a major surface of said semiconductor body of said thyristor.

28. The process of claim 26, including the steps of connecting a plurality of said switching devices fabricated by said integrated circuit process technology distinct from the process technology by which said thyristor is formed between said one of said cathode and anode electrodes and said gate electrode of said thyristor.

29. The process of claim 28, wherein the step of connecting said plurality of said switching devices between said one of said cathode and anode electrodes and said gate electrode of said thyristor includes locating each of said plurality of said switching devices relative to said thyristor such that electrical leads connecting said plurality of said switching devices between said one of said cathode and anode electrodes and said gate electrode of said thyristor are of near-minimum length.

30. The process of claim 28, wherein the step of connecting said plurality of said switching devices is performed to enable them to be switched simultaneously from the high-resistance off state to the low-resistance on state of the respective switching device for turning said thyristor to its off state.

* * * * *